	L #	Hits	Search Text	DBs
1	L1	181	(result meaning) near10 decod$3 near10 (instruction command) near20 (depend$3 based alter$3 modif$6 chang$3 select$5)	EPO; JPO; DERWENT; IBM_TDB
2	L2	109	1 near20 (value data content memory storage register flag)	EPO; JPO; DERWENT; IBM_TDB
3	L3	681	(result meaning) near10 decod$3 near10 (instruction command) near20 (depend$3 based alter$3 modif$6 chang$3 select$5)	USPAT; US-PGPUB
4	L4	430	3 near20 (value data content memory storage register flag)	USPAT; US-PGPUB
5	L5	120	(result meaning) near10 decod$3 near10 (instruction command) near20 (depend$3 based alter$3 modif$6 chang$3)	EPO; JPO; DERWENT; IBM_TDB
6	L8	35	2 not 5	EPO; JPO; DERWENT; IBM_TDB
7	L9	429	(result meaning) near10 decod$3 near10 (instruction command) near20 (depend$3 based alter$3 modif$6 chang$3)	USPAT; US-PGPUB
8	L10	163	4 not 9	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	JP 2003249096 A	☐	SEMICONDUCTOR MEMORY DEVICE	
2	JP 2000347858 A	☒	MICROPROCESSOR	
3	JP 11212804 A	☒	VIRTUAL MACHINE AND PROGRAM CONVERTING DEVICE	
4	JP 11065839 A	☒	INSTRUCTION CONTROL MECHANISM OF PROCESSOR	
5	JP 08328859 A	☒	VIRTUAL PARALLEL ARITHMETIC UNIT APPLIED TO VLIW COMPUTER	
6	JP 08077003 A	☒	DSP PROGRAM PARALLEL PROCESS CONTROLLER	
7	JP 08069407 A	☒	PROCESSOR WITH DATA MEMORY	
8	JP 06337783 A	☒	PROCESSOR AND METHOD FOR DATA PROCESSING	
9	JP 06030064 A	☒	DATA RECEIVER	
10	JP 05341994 A	☒	INSTRUCTION PROCESSING SYSTEM AND DATA PROCESSOR	
11	JP 05233284 A	☒	INSTRUCTION PREFETCH SYSTEM	
12	JP 05046384 A	☒	PIPELINE CONTROL SYSTEM	
13	JP 04054638 A	☒	ELECTRONIC COMPUTER	
14	JP 04021128 A	☒	INSTRUCTION READING CIRCUIT	
15	JP 03196348 A	☒	MEMORY CONTROL CIRCUIT	
16	JP 02118833 A	☒	INSTRUCTION DECODER	
17	JP 02019927 A	☒	DATA PROCESSOR	
18	JP 01008457 A	☒	CONTROL DEVICE FOR STORAGE DEVICE CONSTITUTION	
19	JP 63137330 A	☒	MICROPROGRAM CONTROLLER	
20	JP 62186331 A	☒	RANDOM NUMBER GENERATING CIRCUIT	
21	JP 62070954 A	☒	INFORMATION PROCESSOR	
22	JP 61165148 A	☒	TABLE ACCESS INSTRUCTING SYSTEM	

	Document ID	U	Title	Current OR
23	JP 60039 223 A	☒	MICROCOMPUTER DEVICE	
24	JP 57176 455 A	☒	MICROPROGRAM CONTROL INFORMATION PROCESSOR	
25	JP 57048 139 A	☒	MICROPROGRAM CONTROL DEVICE	
26	JP 56147 245 A	☒	MICROPROGRAM CONTROL DEVICE	
27	JP 56074 751 A	☒	TEST SYSTEM	
28	EP 12715 51 A2	☒	Semiconductor memory device and information device	
29	JP 20031 67730 A	☒	Command set variable microprocessor has programmable logic with command decoder which decodes command to select designated register from register file	
30	EP 12715 51 A	☒	Semiconductor memory for computer, includes command state machine which decodes input command for controlling either status switching circuit or data switching circuit	
31	CN 13000 05 A	☒	Data correlation discriminating and selectively transfering circuit for cnetral processor or microcontroller	
32	EP 75623 0 A	☒	Address setting unit for selecting signal processing instructions in ADPCM system using ROM with conditional branching - has ALU for calculating contents of register file from instruction decoder output for result register, address unit for calculating next instruction ROM address and selector for deciding upon next instruction address	
33	JP 08077 003 A	☒	DSP program parallel control device for portable telephone - performs parallel execution of instructions of third instruction register within same processing period of second instruction register	
34	US 52127 80 A	☒	System for single cycle transfer of unmodified data in memory - includes RAM subarrays having add and even memory locations and data move instruction resulting in externally generated row and column address signals	
35	SU 14447 90 A	☐	Common memory operational elements interface - uses signal to initiate selected current operational element for states memory indication of result destination	

	Document ID	U	Title	Current OR
1	US 20040027902 A1	☐	Semiconductor device with reduced current consumption in standby state	365/222
2	US 20040027857 A1	☒	Nonvolatile semiconductor memory device allowing high speed data transfer	365/185.11
3	US 20040019773 A1	☒	Illegal instruction processing method and processor	712/244
4	US 20040006685 A1	☒	Processor and instruction control method	712/218
5	US 20040004900 A1	☒	Semiconductor integrated circuit device with embedded synchronous memory precisely operating in synchronization with high speed clock	365/230.06
6	US 20030202385 A1	☒	Method for controlling column decoder enable timing in synchronous semiconductor device and apparatus thereof	365/194
7	US 20030101333 A1	☒	Data processor	712/226
8	US 20030097541 A1	☒	Latency tolerant processing equipment	712/1
9	US 20030097519 A1	☒	Memory subsystem	711/5
10	US 20030093648 A1	☒	Method and apparatus for interfacing a processor to a coprocessor	712/34
11	US 20030084270 A1	☒	System and method for translating non-native instructions to native instructions for processing on a host processor	712/204
12	US 20030072199 A1	☒	Semiconductor memory device	365/200
13	US 20030052802 A1	☒	Method and apparatus for huffman decoding technique	341/65
14	US 20020163845 A1	☒	Semiconductor device with reduced current consumption in standby state	365/222
15	US 20020158271 A1	☒	Semiconductor integrated circuit	257/200
16	US 20020087851 A1	☒	Microprocessor and an instruction converter	712/239
17	US 20020083313 A1	☒	Data processing apparatus with many-operand instruction	712/245

	Document ID	U	Title	Current OR
18	US 20020 08271 4 A1	☒	Processor control apparatus, processor, and processor controlling method	700/1
19	US 20020 08067 7 A1	☒	Semiconductor memory device	365/233
20	US 20020 07832 5 A1	☒	Microcomputer and dividing circuit	712/210
21	US 20020 07307 3 A1	☒	Paralleled content addressable memory search engine	707/2
22	US 20020 04287 1 A1	☒	DATA PROCESSOR HAVING AN INSTRUCTION DECODER	712/212
23	US 20020 04042 6 A1	☒	Execution control apparatus of data driven information processor	712/25
24	US 20020 04037 8 A1	☒	Single instruction multiple data processing	708/232
25	US 20020 02782 3 A1	☒	Semiconductor memory device	365/230 .03
26	US 20020 02654 5 A1	☒	Data processing apparatus of high speed process using memory of low speed and low power consumption	710/56
27	US 20010 05414 0 A1	☒	MICROPROCESSOR INCLUDING AN EFFICIENT IMPLEMENTATION OF EXTREME VALUE INSTRUCTIONS	712/223
28	US 20010 04557 9 A1	☒	Semiconductor device with reduced current consumption in standby state	257/222
29	US 20010 03351 9 A1	☒	Semiconductor memory device	365/201
30	US 20010 03229 6 A1	☒	Data processor	711/128
31	US 66290 99 B2	☒	Paralleled content addressable memory search engine	707/10
32	US 65976 17 B2	☒	Semiconductor device with reduced current consumption in standby state	365/222
33	US 65570 98 B2	☒	Microprocessor including an efficient implementation of extreme value instructions	712/223
34	US 65464 71 B1	☒	Shared memory multiprocessor performing cache coherency	711/148
35	US 65265 00 B1	☒	Data driven type information processing system consisting of interconnected data driven type information processing devices	712/25
36	US 65264 74 B1	☒	Content addressable memory (CAM) with accesses to multiple CAM arrays used to generate result for various matching sizes	711/108

	Document ID	U	Title	Current OR
37	US 6523054 B1	☒	Galois field arithmetic processor	708/492
38	US 6462649 B1	☒	Air bag failure display system and method	340/435
39	US 6449707 B1	☒	Information processing unit, information processing structure unit, information processing structure, memory structure unit and semiconductor memory device	712/14
40	US 6414894 B2	☒	Semiconductor device with reduced current consumption in standby state	365/222
41	US 6401196 B1	☒	Data processor system having branch control and method thereof	712/241
42	US 6397323 B1	☒	Data processor having an instruction decoder	712/212
43	US 6385104 B2	☒	Semiconductor memory device having a test mode decision circuit	365/201
44	US 6343357 B1	☒	Microcomputer and dividing circuit	712/210
45	US 6295597 B1	☒	Apparatus and method for improved vector processing to support extended-length integer arithmetic	712/8
46	US 6282629 B1	☒	Pipelined processor for performing parallel instruction recording and register assigning	712/23
47	US 6282505 B1	☒	Multi-port memory and a data processor accessing the same	703/25
48	US 6272620 B1	☒	Central processing unit having instruction queue of 32-bit length fetching two instructions of 16-bit fixed length in one instruction fetch operation	712/41
49	US 6272596 B1	☒	Data processor	711/128
50	US 6266765 B1	☒	Computer architecture capable of execution of general purpose multiple instructions	712/215
51	US 6263423 B1	☒	System and method for translating non-native instructions to native instructions for processing on a host processor	712/209
52	US 6253308 B1	☒	Microcomputer having variable bit width area for displacement and circuit for handling immediate data larger than instruction word	712/210
53	US 6246388 B1	☒	Display driving circuit for displaying character on display panel	345/98
54	US 6205535 B1	☒	Branch instruction having different field lengths for unconditional and conditional displacements	712/33
55	US 6175945 B1	☒	Reed-Solomon decoder	714/784
56	US 6172918 B1	☒	Semiconductor memory device allowing high-speed operation of internal data buses	365/189.11
57	US 6141746 A	☒	Information processor	712/214
58	US 6131154 A	☒	Microcomputer having variable bit width area for displacement	712/32
59	US 6115806 A	☒	Data processor having an instruction decoder and a plurality of executing units for performing a plurality of operations in parallel	712/210

	Document ID	U	Title	Current OR
60	US 6112299 A	☒	Method and apparatus to select the next instruction in a superscalar or a very long instruction word computer having N-way branching	712/236
61	US 6088770 A	☒	Shared memory multiprocessor performing cache coherency	711/148
62	US 6057877 A	☒	NTSC interference detectors using pairs of comb filters with zero-frequency responses, as for DTV receivers	348/21
63	US 6029244 A	☒	Microprocessor including an efficient implementation of extreme value instructions	712/223
64	US 6026485 A	☒	Instruction folding for a stack-based machine	712/226
65	US 6016555 A	☒	Non-intrusive software breakpoints in a processor instruction execution pipeline	714/35
66	US 5991868 A	☒	Apparatus and method for processing data with a plurality of flag groups	712/32
67	US 5991545 A	☒	Microcomputer having variable bit width area for displacement and circuit for handling immediate data larger than instruction word	712/33
68	US 5983334 A	☒	Superscalar microprocessor for out-of-order and concurrently executing at least two RISC instructions translating from in-order CISC instructions	712/23
69	US 5978822 A	☒	Circuit for rotating, left shifting, or right shifting bits	708/209
70	US 5974533 A	☒	Data processor	712/211
71	US 5969976 A	☒	Division circuit and the division method thereof	708/655
72	US 5951678 A	☒	Method and apparatus for controlling conditional branch execution in a data processor	712/237
73	US 5948053 A	☒	Digital signal processor architecture using signal paths to carry out arithmetic operations	708/522
74	US 5938759 A	☒	Processor instruction control mechanism capable of decoding register instructions and immediate instructions with simple configuration	712/209
75	US 5918045 A	☒	Data processor and data processing system	712/237
76	US 5909565 A	☒	Microprocessor system which efficiently shares register data between a main processor and a coprocessor	712/200
77	US 5903919 A	☒	Method and apparatus for selecting a register bank	711/220
78	US 5854939 A	☒	Eight-bit microcontroller having a risc architecture	712/41
79	US 5848268 A	☒	Data processor with branch target address generating unit	712/233
80	US 5838249 A	☒	Control/supervisory signal transmission/reception system	340/3.55
81	US 5835745 A	☒	Hardware instruction scheduler for short execution unit latencies	712/215
82	US 5828874 A	☒	Past-history filtered branch prediction	712/240

	Document ID	U	Title	Current OR
83	US 5809274 A	☒	Purge control for ON-chip cache memory	712/210
84	US 5771363 A	☒	Single-chip microcomputer having an expandable address area	712/200
85	US 5764573 A	☒	Semiconductor device capable of externally and readily identifying set bonding optional function and method of identifying internal function of semiconductor device	365/189.03
86	US 5761492 A	☒	Method and apparatus for uniform and efficient handling of multiple precise events in a processor by including event commands in the instruction set	712/244
87	US 5761470 A	☒	Data processor having an instruction decoder and a plurality of executing units for performing a plurality of operations in parallel	712/210
88	US 5752064 A	☒	Computer architecture capable of concurrent issuance and execution of general purpose multiple instructions	712/23
89	US 5752061 A	☒	Arrangement of data processing system having plural arithmetic logic circuits	712/43
90	US 5751999 A	☒	Processor and data memory for outputting and receiving data on different buses for storage in the same location	711/167
91	US 5687344 A	☒	Single-chip microcomputer having an expandable address area	711/220
92	US 5682545 A	☒	Microcomputer having 16 bit fixed length instruction format	712/41
93	US 5682491 A	☒	Selective processing and routing of results among processors controlled by decoding instructions using mask value derived from instruction tag and processor identifier	712/209
94	US 5680631 A	☒	Data processor with on-chip cache memory and purge controller responsive to external signal for controlling access to the cache memory	712/207
95	US 5666510 A	☒	Data processing device having an expandable address space	711/220
96	US 5649226 A	☒	Processor having multiple instruction registers	712/1
97	US 5649145 A	☒	Data processor processing a jump instruction	711/213
98	US 5646875 A	☒	Denormalization system and method of operation	708/508
99	US 5636155 A	☒	Arithmetic processor and arithmetic method	708/631
100	US 5619666 A	☒	System for translating non-native instructions to native instructions and combining them into a final bucket for processing on a host processor	712/208
101	US 5619662 A	☒	Memory reference tagging	712/216
102	US 5617550 A	☒	Data processor generating jump target address of a jump instruction in parallel with decoding of the instruction	712/207
103	US 5592637 A	☒	Data processor processing a jump instruction	712/237
104	US 5590296 A	☒	Data processor processing a jump instruction	712/229
105	US 5581719 A	☒	Multiple block line prediction	712/207

	Document ID	U	Title	Current OR
106	US 5579253 A	☒	Computer multiply instruction with a subresult selection option	708/625
107	US 5564118 A	☒	Past-history filtered branch prediction	712/240
108	US 5546552 A	☒	Method for translating non-native instructions to native instructions and combining them into a final bucket for processing on a host processor	712/209
109	US 5519841 A	☒	Multi instruction register mapper	711/202
110	US 5517462 A	☒	Synchronous type semiconductor memory device operating in synchronization with an external clock signal	365/233
111	US 5485587 A	☒	Data processor calculating branch target address of a branch instruction in parallel with decoding of the instruction	712/234
112	US 5453927 A	☒	Data processor for processing branch instructions	712/235
113	US 5440704 A	☒	Data processor having branch predicting function	712/239
114	US 5440702 A	☒	Data processing system with condition code architecture for executing single instruction range checking and limiting operations	712/223
115	US 5438668 A	☒	System and method for extraction, alignment and decoding of CISC instructions into a nano-instruction bucket for execution by a RISC computer	712/204
116	US 5404552 A	☒	Pipeline risc processing unit with improved efficiency when handling data dependency	712/41
117	US 5404338 A	☒	Synchronous type semiconductor memory device operating in synchronization with an external clock signal	365/233
118	US 5349672 A	☒	Data processor having logical address memories and purge capabilities	711/123
119	US 5329611 A	☒	Scalable flow virtual learning neurocomputer	706/42
120	US 5321821 A	☒	System for processing parameters in instructions of different format to execute the instructions using same microinstructions	712/210
121	US 5299320 A	☒	Program control type vector processor for executing a vector pipeline operation for a series of vector data which is in accordance with a vector pipeline	712/231
122	US 5254949 A	☒	Decreasing processing time for type 1 dyadic instructions	712/223
123	US 5220656 A	☒	System for selecting control parameter for microinstruction execution unit using parameters and parameter selection signal decoded from instruction	712/211
124	US 5212780 A	☒	System for single cycle transfer of unmodified data to a next sequentially higher address in a semiconductor memory	365/230.04
125	US 5206945 A	☒	Single-chip pipeline processor for fetching/flushing instruction/data caches in response to first/second hit/mishit signal respectively detected in corresponding to their logical addresses	711/3
126	US 5159598 A	☒	Buffer integrated circuit providing testing interface	714/724
127	US 5129075 A	☒	Data processor with on-chip logical addressing and off-chip physical addressing	711/169

	Document ID	U	Title	Current OR
128	US 5128668 A	☒	Remote-controlled electronic equipment with a transmitting function	340/825.72
129	US 5117382 A	☒	Semiconductor integrated circuit for performing an arithmetic operation including bipolar and MOS transistors	708/490
130	US 5113503 A	☒	Data processor providing plural decoders for effecting fast register selection	712/212
131	US 5031134 A	☒	System for evaluating multiple integrals	708/444
132	US 4992938 A	☒	Instruction control mechanism for a computing system with register renaming, map table and queues indicating available registers	712/217
133	US 4989140 A	☒	Single chip pipeline data processor using instruction and operand cache memories for parallel operation of instruction control and executions unit	711/207
134	US 4975839 A	☒	Instruction decode method and arrangement suitable for a decoder of microprocessors	712/211
135	US 4912635 A	☒	System for reexecuting branch instruction without fetching by storing target instruction control information	712/238
136	US 4897636 A	☒	Video display control system for moving display images	345/682
137	US 4868822 A	☒	Memory emulation method and system for testing and troubleshooting microprocessor-based electronic systems	714/29
138	US 4858105 A	☒	Pipelined data processor capable of decoding and executing plural instructions in parallel	712/235
139	US 4835679 A	☒	Microprogram control system	712/212
140	US 4811203 A	☒	Hierarchial memory system with separate criteria for replacement and writeback without replacement	711/142
141	US 4789958 A	☒	Carry-look-ahead adder including bipolar and MOS transistors	708/710
142	US 4785393 A	☒	32-Bit extended function arithmetic-logic unit on a single chip	712/221
143	US 4752873 A	☒	Data processor having a plurality of operating units, logical registers, and physical registers for parallel instructions execution	712/23
144	US 4736288 A	☒	Data processing device	712/217
145	US 4731742 A	☒	Video display control system	345/572
146	US 4630194 A	☒	Apparatus for expediting sub-unit and memory communications in a microprocessor implemented data processing system having a multibyte system bus that utilizes a bus command byte	710/100
147	US 4564302 A	☒	Control device for printer which has function of format data printing	400/76
148	US 4530055 A	☒	Hierarchical memory system with variable regulation and priority of writeback from cache memory to bulk memory	711/136
149	US 4530054 A	☒	Processor-addressable timestamp for indicating oldest written-to cache entry not copied back to bulk memory	711/133
150	US 4523206 A	☒	Cache/disk system with writeback regulation relative to use of cache memory	711/130

	Document ID	U	Title	Current OR
151	US 4426646 A	☒	Self shift type gas discharge panel, driving system	345/62
152	US 4303978 A	☒	Integrated-strapdown-air-data sensor system	701/220
153	US RE30679 E	☒	Character generating method and system	345/472
154	US 4100597 A	☒	Computer controlled distribution apparatus for distributing transactions to and from controlled machine tools having means independent of the computer for completing or stopping a tool function initiated by a computer transaction	700/169
155	US 4069488 A	☒	Computer controlled distribution apparatus for distributing transactions to and from controlled machines tools	700/169
156	US 4029947 A	☒	Character generating method and system	345/472
157	US 4001568 A	☒	Monetary receipt and payment managing apparatus	705/43
158	US 3996565 A	☒	Programmable sequence controller	700/9
159	US 3849765 A	☒	PROGRAMMABLE LOGIC CONTROLLER	712/246
160	US 3793631 A	☒	DIGITAL COMPUTER APPARATUS OPERATIVE WITH JUMP INSTRUCTIONS	712/233
161	US 3753246 A	☒	PRINTER ADAPTED FOR OPERATION WITH A PROGRAMMABLE CONTROLLER	358/1.15
162	US 3676846 A	☒	MESSAGE BUFFERING COMMUNICATION SYSTEM	714/749
163	US 3591786 A	☐	PREDICTED ITERATION IN DECIMAL DIVISION	708/652

	L #	Hits	Search Text	DBs
1	L1	429	(result meaning) near10 decod$3 near10 (instruction command) near20 (depend$3 based alter$3 modif$6 chang$3)	USPAT; US-PGPUB
2	L3	120	(result meaning) near10 decod$3 near10 (instruction command) near20 (depend$3 based alter$3 modif$6 chang$3)	EPO; JPO; DERWENT; IBM_TDB
3	L2	260	1 near20 (value data content memory storage register flag)	USPAT; US-PGPUB
4	L5	74	3 near20 (value data content memory storage register flag)	EPO; JPO; DERWENT; IBM_TDB
5	L6	169	1 not 2	USPAT; US-PGPUB
6	L7	46	3 not 5	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	JP 2003242799 A	☐	SEMICONDUCTOR INTEGRATED CIRCUIT	
2	JP 2002014809 A	☒	MICROPROCESSOR AND ASSEMBLER AND ITS METHOD AND RECORDING MEDIUM WITH ITS PROGRAM RECORDED	
3	JP 2001344100 A	☒	CENTRAL PROCESSING UNIT EQUIPPED WITH PLURAL FLAG REGISTERS	
4	JP 2001175470 A	☒	DATA PROCESSOR	
5	JP 2000137619 A	☒	MICROCOMPUTER	
6	JP 11177653 A	☒	MPEG DATA MSFER CONTROL CIRCUIT	
7	JP 11136207 A	☒	RECEPTION SIGNAL CORRECTION SYSTEM AND ORTHOGONAL FREQUENCY DIVISION MULTIPLEX SIGNAL TRANSMITTER	
8	JP 11031105 A	☒	DEVICE AND METHOD FOR PRODUCING DATA CAPSULE	
9	JP 11015590 A	☒	PERSONAL COMPUTER SYSTEM	
10	JP 10224147 A	☒	FREQUENCY-ADJUSTING DEVICE OF OSCILLATOR CIRCUIT	
11	JP 10224146 A	☒	FREQUENCY-ADJUSTING DEVICE FOR OSCILLATOR CIRCUIT	
12	JP 10105396 A	☒	PROCESSOR	
13	JP 10050055 A	☒	SEMICONDUCTOR MEMORY AND DATA PROCESSOR	
14	JP 09311786 A	☒	DATA PROCESSOR	
15	JP 08222996 A	☒	AUTOMATIC CHANNEL SELECTION METHOD FOR RADIO BROADCAST	
16	JP 08153000 A	☒	INSTRUCTION PROCESSOR	
17	JP 07154677 A	☒	IMAGE PICKUP DEVICE	
18	JP 06290078 A	☒	MICROPROCESSOR	
19	JP 05265912 A	☒	COMMAND CODE ISSUING METHOD	
20	JP 05252119 A	☒	SAMPLING FREQUENCY CONVERTER	
21	JP 05224928 A	☒	DATA PROCESSOR	

	Document ID	U	Title	Current OR
22	JP 05165 629 A	☒	MICROPROCESSOR	
23	JP 05012 010 A	☒	BRANCH FORECAST SYSTEM	
24	JP 05012 008 A	☒	CENTRAL ARITHMETIC PROCESSING UNIT	
25	JP 04353 925 A	☒	ARITHMETIC UNIT	
26	JP 04328 644 A	☒	DEBUG BACK-UP DEVICE	
27	JP 04288 688 A	☒	BIT MAP DISPLAY CONTROLLER	
28	JP 04273 529 A	☒	PARALLEL ARITHMETIC CIRCUIT	
29	JP 04162 156 A	☒	INFORMATION PROCESSOR	
30	JP 04062 637 A	☒	MICROPROCESSOR	
31	JP 04035 180 A	☒	REPRODUCTION INFORMATION DISPLAY DEVICE	
32	JP 04000 515 A	☒	CLOCK SUPPLYING SYSTEM AND ARITHMETIC PROCESSOR	
33	JP 03149 622 A	☒	DATA PROCESSOR	
34	JP 03132 843 A	☒	MICROPROCESSOR	
35	JP 03095 629 A	☒	DATA PROCESSOR	
36	JP 01309 129 A	☒	MICROPROCESSOR	
37	JP 01261 780 A	☒	STORAGE CONTROL SYSTEM	
38	JP 01106 244 A	☒	VIRTUAL STORAGE DEVICE	
39	JP 01036 334 A	☒	MICROCOMPUTER	
40	JP 63208 142 A	☒	INFORMATION PROCESSOR	
41	JP 63036 432 A	☒	FLOATING POINT ARITHMETIC UNIT	
42	JP 62285 137 A	☒	DIGITAL SIGNAL PROCESSOR	
43	JP 62224 828 A	☒	INFORMATION PROCESSOR	
44	JP 62119 638 A	☒	DATA PROCESSING SYSTEM	

	Document ID	U	Title	Current OR
45	JP 62044834 A	☒	CONTROL SYSTEM FOR ELECTRONIC COMPUTER	
46	JP 60114972 A	☒	FORM FORMAT FORMING DEVICE	
47	JP 56074749 A	☒	MICROPROGRAM CONTROLLING DEVICE	
48	WO 9813759 A1	☒	DATA PROCESSOR AND DATA PROCESSING SYSTEM	
49	JP 2003085509 A	☒	Memory card for personal computer, has process unit that detects whether received command is effective, based on decoding result of command and set index value	
50	US 20020174300 A	☒	Data processor pre-codes advanced instruction portion of instruction data before instruction data is processed and loads instruction codes required for processing into cache memory based on pre-decoding results	
51	EP 1168129 A	☒	Microcontroller with variable instruction coding has decoder designed to decode at least one conditional instruction so result of decoding this instruction depends on contents of memory	
52	JP 2001344100 A	☒	Central processing unit stores condition of calculation result of decoded input command in several flag registers whose branch conditions are judged based on stored result	
53	JP 2001265751 A	☒	Microcomputer device for mobile-communication apparatus, changes operation condition of device based on command data decoding result	
54	WO 2001402903 A	☒	Data processing apparatus for executing specific load instruction in which converter circuit converts integer data whose bit length is shorter than bit length of floating-point data register	
55	JP 2001109626 A	☒	Pipeline calculating unit in computer system, has instruction decoder decoding instructions published to calculator to store result in downstream latch based on data held by upstream latch	
56	JP 2001014160 A	☒	Information processor for pipeline architecture, outputs instruction reading demand to memory based on result of preset instruction decoder	
57	JP 11275205 A	☒	Aural command based telephone number dialing system in telephone - has speech recognition unit which recognizes decoded input phonation among stored results and displays best decoding result for dial operation	
58	JP 11232170 A	☒	Instruction memory extension apparatus for semiconductor device - has memory control unit for memory operation, based on starting signal and memory extension control unit for memory space based on completion instruction	
59	JP 11191088 A	☒	External auxiliary memory for computer system - has two device bus control units which respectively access data unit depending on decoding result from two input output command process units	
60	JP 11154393 A	☒	Non-volatile semiconductor memory e.g. electrically erasable programmable read only memory EEPROM, used for recording of multimedia information - has controller which makes predetermined number as designated page unit when predetermined command for designating program unit is included based on decoding result of command decoder	
61	JP 11024929 A	☒	Calculation processing apparatus - has selector that chooses one instruction from simultaneously fetched instructions, and outputs chosen instruction to decoder based on decision result of branch conditions about branch instruction	
62	US 5826097 A	☒	Data driven information processing - involves subjecting data packets to specified operation processing based on its decoded instruction result and adding operation processing results, cumulatively	

	Document ID	U	Title	Current OR
63	JP 10161871 A	☒	Processor architecture e.g. for microprocessor, signal processor - has instruction decoder which outputs control signal to forward data depending on condition judging result, when input instruction is data forwarding instruction	
64	WO 9813759 A	☒	Data processor and data processing system - provides task buffers with program storage area and pointer for successively reading out instructions selected through selector, and controls selection by switching controller in accordance with internally or externally-generated event	
65	JP 10050055 A	☒	Semiconductor memory for computer system, e.g. SGRAM - has input data controllers which facilitate simultaneous write-in of data in several column addresses of memory cell array based on decoded form of data block write command	
66	JP 08241296 A	☒	semiconductor IC with built-in synchronous memory for processing data - has precharge control part which deters generation of precharge demand signal, when first and second prohibition signals show that decoding result is invalid	
67	EP 582991 A	☒	Data processing circuit with CPU and inbuilt electrically rewritable non-volatile flash memory in single substrate - includes command latch made externally writable, command analyser and sequence controller	
68	EP 561271 A	☒	Microcomputer with non-volatile flash memory with writable information - has central processor with multiple memory blocks of different capacities, switched between operation modes when rewriting memory	
69	EP 417013 A	☒	Data processor decoding and executing train of instructions - stores prefetched instruction code, and sequentially outputs instruction with units of set number of bits	
70	SU 1628215 A	☒	Transceiver for communication engineering - has signal input of error analyser on transmission side connected to error output of decoder and signal input of matching unit	
71	EP 399762 A	☒	Multiple instruction issue computer architecture - has series of pipeline stages and includes resources for accepting family of instructions at each stage	
72	EP 374370 A	☒	Non exclusive cache lines storage in multiprocessor systems - by allowing instruction execution to continue without result commitment until cache line made exclusive	
73	EP 301220 A	☒	Computer system allowing out of sequence instruction execution - executes instruction register array using processor store and hardware register	
74	SU 1176334 A	☐	Programmes and micro-programmes tester - has input taken via OR=gates to address counter with output taken to memory and register	

	Document ID	U	Title	Current OR
1	JP 2001184231 A	☐	PROGRAM DEVELOPMENT SUPPORTING DEVICE AND METHOD OF CONTROLLING THE SAME	
2	JP 2000099329 A	☒	PROCESSOR	
3	JP 11283295 A	☒	MAGNETIC RECORDING/REPRODUCING DEVICE	
4	JP 11154393 A	☒	NON-VOLATILE SEMICONDUCTOR MEMORY	
5	JP 10228421 A	☒	MEMORY ACCESS CONTROL CIRCUIT	
6	JP 10164511 A	☒	MICROPROCESSOR AND VIDEO INFORMATION PROCESSING SYSTEM	
7	JP 10031588 A	☒	ARITHMETIC UNIT AND ITS DESIGNING METHOD	
8	JP 09282163 A	☒	DOUBLE INSTRUCTION FETCH PROCESSOR	
9	JP 09172598 A	☒	SERVER/CLIENT SYSTEM AND DATA TRANSFER SYSTEM	
10	JP 08095784 A	☒	PROCESSOR AND METHOD FOR ARITHMETIC PROCESSING	
11	JP 07250375 A	☒	DIGITAL DATA COMMUNICATION ADAPTOR	
12	JP 07154743 A	☒	HIGH-SPEED IMAGE REPRODUCING SYSTEM	
13	JP 05268546 A	☒	VOICE DECODER CIRCUIT CONTROLLER	
14	JP 05127892 A	☒	INSTRUCTION EXECUTING SYSTEM	
15	JP 05066939 A	☒	BLOCK OPERATING INSTRUCTION EXECUTING DEVICE FOR INTEGRATED CIRCUIT MICROPROCESSOR	
16	JP 05013851 A	☒	LIGHT TRANSMITTING EQUIPMENT	
17	JP 04336791 A	☒	ELECTRONIC METER AUTOMATIC INSPECTION SYSTEM	
18	JP 04098426 A	☒	MICROPROCESSOR	
19	JP 04054636 A	☒	PROCESSOR	
20	JP 03077137 A	☒	INFORMATION PROCESSOR	
21	JP 03053324 A	☒	PROGRAM LOOP CONTROL SYSTEM	
22	JP 02130635 A	☒	SIMULTANEOUS PROCESSING SYSTEM FOR PLURAL INSTRUCTIONS	

	Document ID	U	Title	Current OR
23	JP 63093 036 A	☒	SECRECY HOLDING SYSTEM FOR 1-CHIP MICROCOMPUTER	
24	JP 63006 658 A	☒	FORME SYSTEM	
25	JP 61294 557 A	☒	INSTRUCTION PROCESSOR	
26	JP 58003 013 A	☒	CHANNEL CONTROLLING SYSTEM	
27	JP 55049 751 A	☒	MICROPROGRAM CONTROL UNIT	
28	WO 99211 22 A1	☒	VOICE-OUTPUT READING SYSTEM WITH GESTURE-BASED NAVIGATION	
29	EP 43720 7 A2	☒	Information processing system.	
30	EP 41701 3 A2	☒	Data processor decoding and executing a train of instructions of variable length.	
31	EP 37437 0 A2	☒	Method for storing into non-exclusive cache lines in multiprocessor systems.	
32	CN 13491 60 A	☒	Correlation delay eliminating method for streamline control	
33	JP 20020 73328 A	☒	Digital signal processor judges execution of lower order instruction word, based on the decoding results obtained with respect to previous execution	
34	JP 20010 34471 A	☒	Very large instruction word system processor used in multimedia fields, executes branch inspection when calculation instruction processing is irrespective of output of instruction decoder	
35	JP 20002 07209 A	☒	Arithmetic logic unit of very long instruction word processor system, performs various calculations based on decoding result of program and clock supply units respectively supply clock signals for operating ALUs	
36	JP 20001 37619 A	☒	Signal chip microcomputer consists of instruction decoding circuit which decodes instruction fetched from program memory based on instruction decipherment mode judged by interruption control circuit	
37	US 60584 71 A	☒	Data processing system includes sub decoder and main decoder which are prevented from decoding instruction other than respective instruction in instruction set	
38	JP 20000 99329 A	☒	Processor used for instruction pipeline processing, includes arithmetic logic units which are controlled based on decoded operation indication results	
39	JP 11283 295 A	☒	Magnetic tape drive speed controller used in VTR - superimposes magnetic tape management information on control signal and decodes it, based on identification result of CTL duty ratio and thereby controls recording command validation	
40	JP 10254 725 A	☒	Information processor - has rubble circuit which is rearranged when certain predetermined conditions are satisfied by executing instruction	
41	JP 10161 873 A	☒	Microprocessor with instruction decoding function - performs conditional branch operation based on condition signal depending on execution of instruction prior to conditional branch instruction	
42	US 55600 36 A	☒	Data processor with emulation function for system debugging - includes operand access control unit, receiving operand data and control values to prevent or permit access to high speed store for operand transfer	

	Document ID	U	Title	Current OR
43	JP 07320488 A	☒	Batch erasure method for non-volatile memory device - involves fourth motion doing low speed erasure of small reference threshold voltage according to lump energy of non-volatile element at each erasure	
44	DE 4134392 A	☒	parallel processor for several commands - has functional units, commad memory and recall, and decoder for command recognition	
45	EP 437207 A	☒	Information processing system - has execution unit which include flag register and buffer with ALU reading state held in register and buffer	
46	EP 417587 A	☐	Data processor with check for undefined addresses - has decoder generating flag for input to detector stage	

	L #	Hits	Search Text	DBs
1	L1	429	(result meaning) near10 decod$3 near10 (instruction command) near20 (depend$3 based alter$3 modif$6 chang$3)	USPAT; US-PGPUB
2	L2	260	1 near20 (value data content memory storage register flag)	USPAT; US-PGPUB
3	L3	120	(result meaning) near10 decod$3 near10 (instruction command) near20 (depend$3 based alter$3 modif$6 chang$3)	EPO; JPO; DERWENT; IBM_TDB
4	L5	74	3 near20 (value data content memory storage register flag)	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	US 20040025000 A1	☐	Multistandard video decoder and decompression system for processing encoded bit streams including start code detection and methods relating thereto	712/300
2	US 20040019775 A1	☒	Multistandard video decoder and decompression system for processing encoded bit streams including tokens and methods relating thereto	712/300
3	US 20040015680 A1	☒	Data processor for modifying and executing operation of instruction code	712/226
4	US 20040008788 A1	☒	MPEG video decoder and MPEG video decoding method	375/240.25
5	US 20040003214 A1	☒	Instruction control method and processor	712/234
6	US 20040003207 A1	☒	Program counter control method and processor	712/218
7	US 20030227969 A1	☒	Multistandard video decoder and decompression system for processing encoded bit streams including a reconfigurable processing stage and methods relating thereto	375/240.1
8	US 20030214850 A1	☒	Non-volatile multi-level semiconductor flash memory device and method of driving same	365/199
9	US 20030204652 A1	☒	Data transfer control device, electronic equipment and data transfer control method	710/33
10	US 20030200237 A1	☒	Serial operation pipeline, arithmetic device, arithmetic-logic circuit and operation method using the serial operation pipeline	708/233
11	US 20030196078 A1	☒	Data pipeline system and data encoding method	712/300
12	US 20030191599 A1	☒	Method and protocol tester for decoding data encoded in accordance with a protocol description	702/100
13	US 20030182589 A1	☒	Instruction conversion apparatus and instruction conversion method providing power control information, program and circuit for implementing the instruction conversion, and microprocessor for executing the converted instruction	713/300
14	US 20030182544 A1	☒	Multistandard video decoder and decompression system for processing encoded bit streams including a decoder with token generator and methods relating thereto	712/300
15	US 20030174077 A1	☒	Method of performing huffman decoding	341/67
16	US 20030163606 A1	☒	High-speed memory system	710/1
17	US 20030156652 A1	☒	Multistandard video decoder and decompression system for processing encoded bit streams including a video formatter and methods relating thereto	375/240.26

	Document ID	U	Title	Current OR
18	US 20030151962 A1	☒	Semiconductor integrated circuit device	365/201
19	US 20030144755 A1	☒	Method for processing and reproducing audio signal at desired sound quality, reduced data volume or adjusted output level, apparatus for processing audio signal with sound quality control information or test tone signal or at reduced data volume, recording medium for recording audio signal with sound quality control information or test tone signal or at reduced data volume, and apparatus for reproducing audio signal at desired sound quality, reduced data volume or adjusted output level	700/94
20	US 20030142570 A1	☒	Memory controller and serial memory	365/221
21	US 20030123297 A1	☒	Fast cycle RAM having improved data write operation	365/189.05
22	US 20030117843 A1	☒	Non-volatile multi-level semiconductor flash memory device and method of driving same	365/185.03
23	US 20030093652 A1	☒	Operand file using pointers and reference counters and a method of use	712/217
24	US 20030085821 A1	☒	Method of performing Huffman decoding	341/65
25	US 20030079117 A1	☒	Multistandard video decoder and decompression method for processing encoded bit streams according to respective different standards	712/300
26	US 20030066018 A1	☒	Apparatus and method for stopping iterative decoding in a CDMA mobile communication system	714/792
27	US 20030065911 A1	☒	Data processor	712/227
28	US 20030056088 A1	☒	Processor, compiler and compilation method	712/214
29	US 20030043670 A1	☒	Memory control apparatus for serial memory	365/221
30	US 20030042523 A1	☒	Semiconductor integrated circuit device having link element	257/298
31	US 20030037342 A1	☒	Video encoding scheme supporting the transport of audio and auxiliary information	725/146
32	US 20030035485 A1	☒	Data separation and decoding device	375/240.25
33	US 20030028733 A1	☒	Memory apparatus	711/154

	Document ID	U	Title	Current OR
34	US 20030026342 A1	☒	Decoding apparatus, decoding method, decoding program, and decoding program storage medium	375/240.25
35	US 20030021163 A1	☒	Semiconductor memory device and information device	365/189.12
36	US 20030018884 A1	☒	Multistandard video decoder and decompression system for processing encoded bit streams including expanding run length codes and methods relating thereto	712/300
37	US 20030016550 A1	☒	Semiconductor memory systems, methods, and devices for controlling active termination	365/63
38	US 20030005011 A1	☒	Sticky z bit	708/490
39	US 20030004588 A1	☒	Method for processing and reproducing audio signal at desired sound quality, reduced data volume or adjusted output level, apparatus for processing audio signal with sound quality control information or test tone signal or at reduced data volume, recording medium for recording audio signal with sound quality control information or test tone signal or at reduced data volume, and apparatus for reproducing audio signal at desired sound quality, reduced data volume or adjusted output level	700/94
40	US 20020186892 A1	☒	Method and apparatus for coding of wavelet transformed coefficients	382/240
41	US 20020174300 A1	☒	Data processor and data processing method	711/123
42	US 20020152369 A1	☒	Multistandard video decoder and decompression system for processing encoded bit streams including storing data and methods relating thereto	712/300
43	US 20020128739 A1	☒	Method for processing and reproducing audio signal at desired sound quality, reduced data volume or adjusted output level, apparatus for processing audio signal with sound quality control information or test tone signal or at reduced data volume, recording medium for recording audio signal with sound quality control information or test tone signal or at reduced data volume, and apparatus for reproducing audio signal at desired sound quality, reduced data volume or adjusted output level	700/94
44	US 20020123810 A1	☒	Method for processing and reproducing audio signal at desired sound quality, reduced data volume or adjusted output level, apparatus for processing audio signal with sound quality control information or test tone signal or at reduced data volume, recording medium for recording audio signal with sound quality control information or test tone signal or at reduced data volume, and apparatus for reproducing audio signal at desired sound quality, reduced data	700/94
45	US 20020122482 A1	☒	Method of performing video encoding rate control using bit budget	375/240.03
46	US 20020118746 A1	☒	Method of performing video encoding rate control using motion estimation	375/240.03
47	US 20020085633 A1	☒	Method of performing video encoding rate control	375/240.03

	Document ID	U	Title	Current OR
48	US 20020080649 A1	☒	Non-volatile multi-level semiconductor flash memory device and method of driving same	365/185.03
49	US 20020078294 A1	☒	HIGH-SPEED RANDOM ACCESS SEMICONDUCTOR MEMORY DEVICE	711/105
50	US 20020066007 A1	☒	Multistandard video decoder and decompression system for processing encoded bit streams including pipeline processing and methods relating thereto	712/300
51	US 20020065574 A1	☒	Data processor, semiconductor integrated circuit and CPU	700/121
52	US 20020046372 A1	☒	SEQUENCE CONTROL CIRCUIT	714/718
53	US 20020040430 A1	☒	Microcontroller	712/234
54	US 20020013872 A1	☒	Synchronous signal producing circuit for controlling a data ready signal indicative of end of access to a shared memory and thereby controlling synchronization between processor and coprocessor	710/240
55	US 20020002670 A1	☒	DATA PROCESSING DEVICE	712/245
56	US 20010043345 A1	☒	Object optimized printing system and method	358/1.9
57	US 20010024205 A1	☒	Graphic processor and graphic processing system	345/520
58	US 20010013095 A1	☒	MICROPROCESSOR HAVING DELAYED INSTRUCTIONS	712/234
59	US 20010007541 A1	☒	Semiconductor memory device	365/233
60	US 20010005132 A1	☒	Semiconductor device testing method and system and recording medium	324/158.1
61	US 20010005012 A1	☒	Fast cycle ram having improved data write operation	257/1
62	US 20010004756 A1	☒	Instruction processing apparatus	712/217
63	US 6671064 B2	☒	Object optimized printing system and method	358/1.15
64	US 6639863 B2	☒	Semiconductor integrated circuit device having link element	365/225.7
65	US 6636445 B2	☒	Fast cycle ram having improved data write operation	365/190

	Document ID	U	Title	Current OR
66	US 6628719 B1	☒	MPEG video decoder and MPEG video decoding method	375/240.28
67	US 6617842 B2	☒	Semiconductor device testing method and system employing trace data	324/158.1
68	US 6615339 B1	☒	VLIW processor accepting branching to any instruction in an instruction word set to be executed consecutively	712/24
69	US 6608823 B1	☒	CDMA mobile communication system and service area	370/331
70	US 6604193 B1	☒	Processor in which register number translation is carried out	712/228
71	US 6590808 B1	☒	Non-volatile multi-level semiconductor flash memory device and method of driving same	365/185.03
72	US 6563439 B1	☒	Method of performing Huffman decoding	341/65
73	US 6560497 B2	☒	METHOD FOR PROCESSING AND REPRODUCING AUDIO SIGNAL AT DESIRED SOUND QUALITY, REDUCED DATA VOLUME OR ADJUSTED OUTPUT LEVEL, APPARATUS FOR PROCESSING AUDIO SIGNAL WITH SOUND QUALITY CONTROL INFORMATION OR TEST TONE SIGNAL OR AT REDUCED DATA VOLUME, RECORDING MEDIUM FOR RECORDING AUDIO SIGNAL WITH SOUND QUALITY CONTROL INFORMATION OR TEST TONE SIGNAL OR AT REDUCED DATA VOLUME, AND APPARATUS FOR REPRODUCING AUDIO SIGNAL AT DESIRED SOUND QUALITY, REDUCED DATA VOLUME OR ADJUSTED OUTPUT LEVEL	700/94
74	US 6549475 B2	☒	Semiconductor memory device and information device	365/189.12
75	US 6539356 B1	☒	Signal encoding and decoding method with electronic watermarking	704/270
76	US 6535984 B1	☒	Power reduction for multiple-instruction-word processors with proxy NOP instructions	713/320
77	US 6535972 B1	☒	Shared dependency checking for status flags	712/217
78	US 6532530 B1	☒	Data processing system and method for performing enhanced pipelined operations on instructions for normal and specific functions	712/35
79	US 6516391 B1	☒	Multiprocessor system and methods for transmitting memory access transactions for the same	711/146
80	US 6504789 B2	☒	Semiconductor memory device	365/233
81	US 6502186 B2	☒	Instruction processing apparatus	712/217
82	US 6496919 B1	☒	Data processor	712/24
83	US 6496411 B2	☒	Non-volatile multi-level semiconductor flash memory device and method of driving same	365/185.03
84	US 6480297 B1	☒	Image forming apparatus	358/1.16
85	US 6442701 B1	☒	Power saving by disabling memory block access for aligned NOP slots during fetch of multiple instruction words	713/324
86	US 6438680 B1	☒	Microprocessor	712/210

	Document ID	U	Title	Current OR
87	US 6435737 B1	☒	Data pipeline system and data encoding method	712/200
88	US 6429948 B1	☒	Object optimized printing system and method	358/1.15
89	US 6427205 B1	☒	Digital signal processor and processor reducing the number of instructions upon processing condition execution instructions	712/226
90	US 6425047 B1	☒	Process containing address decoders suited to improvements in clock speed	711/101
91	US 6421773 B1	☒	Sequence control circuit	712/234
92	US 6385084 B1	☒	Semiconductor memory	365/185.03
93	US 6378061 B1	☒	Apparatus for issuing instructions and reissuing a previous instructions by recirculating using the delay circuit	712/200
94	US 6377862 B1	☒	Method for processing and reproducing audio signal	700/94
95	US 6356508 B1	☒	Semiconductor storage device	365/233
96	US 6335878 B1	☒	Non-volatile multi-level semiconductor flash memory device and method of driving same	365/185.03
97	US 6330666 B1	☒	Multistandard video decoder and decompression system for processing encoded bit streams including start codes and methods relating thereto	712/300
98	US 6330565 B1	☒	Video parser	712/300
99	US 6327043 B1	☒	Object optimized printing system and method	358/1.15
100	US 6324639 B1	☒	Instruction converting apparatus using parallel execution code	712/212
101	US 6292863 B1	☒	PC card	710/313
102	US 6282633 B1	☒	High data density RISC processor	712/208
103	US 6282632 B1	☒	Information processor having duplicate operation flags	712/42
104	US 6263422 B1	☒	Pipeline processing machine with interactive stages operable in response to tokens and system and methods relating thereto	712/209
105	US 6256104 B1	☒	Object optimized printing system and method	358/1.15
106	US 6239829 B1	☒	Systems and methods for object-optimized control of laser power	347/251
107	US 6229543 B1	☒	Microprocessor, and graphics processing apparatus and method using the same	345/418
108	US 6219779 B1	☒	Constant reconstructing processor which supports reductions in code size	712/210
109	US 6198767 B1	☒	Apparatus for color component compression	375/240.01

	Document ID	U	Title	Current OR
110	US 6170082 B1	☒	Taking corrective action in computer programs during instruction processing	717/127
111	US 6166950 A	☒	Nonvolatile semiconductor storage device	365/185.03
112	US 6161171 A	☒	Apparatus for pipelining sequential instructions in synchronism with an operation clock	712/42
113	US 6157997 A	☒	Processor and information processing apparatus with a reconfigurable circuit	712/226
114	US 6157996 A	☒	Processor programably configurable to execute enhanced variable byte length instructions including predicated execution, three operand addressing, and increased register space	712/218
115	US 6157995 A	☒	Circuit and method for reducing data dependencies between instructions	712/25
116	US 6131158 A	☒	Data processing system capable of executing groups of instructions, including at least one arithmetic instruction, in parallel	712/244
117	US 6112017 A	☒	Pipeline processing machine having a plurality of reconfigurable processing stages interconnected by a two-wire interface bus	712/200
118	US 6108793 A	☒	Semiconductor device having timing-stabilization circuit and method of testing such semiconductor device	713/400
119	US 6092183 A	☒	Data processor for processing a complex instruction by dividing it into executing units	712/215
120	US 6079009 A	☒	Coding standard token in a system compromising a plurality of pipeline stages	712/209
121	US 6072832 A	☒	Audio/video/computer graphics synchronous reproducing/synthesizing system and method	375/240.28
122	US 6067417 A	☒	Picture start token	712/18
123	US 6058471 A	☒	Data processing system capable of executing groups of instructions in parallel	712/212
124	US 6047112 A	☒	Technique for initiating processing of a data stream of encoded video information	714/1
125	US 6044455 A	☒	Central processing unit adapted for pipeline process	712/213
126	US 6041387 A	☒	Apparatus for read/write-access to registers having register file architecture in a central processing unit	711/5
127	US 6038380 A	☒	Data pipeline system and data encoding method	712/200
128	US 6035126 A	☒	Data pipeline system and data encoding method	712/29
129	US 6026480 A	☒	Processor having bug avoidance function and method for avoiding bug in processor	712/37
130	US 6023757 A	☒	Data processor	712/209
131	US 6018776 A	☒	System for microprogrammable state machine in video parser clearing and resetting processing stages responsive to flush token generating by token generator responsive to received data	710/7

	Document ID	U	Title	Current OR
132	US 6016543 A	☒	Microprocessor for controlling the conditional execution of instructions	712/233
133	US 6012141 A	☒	Apparatus for detecting and executing traps in a superscalar processor	712/244
134	US 6006322 A	☒	Arithmetic logic unit and microprocessor capable of effectively executing processing for specific application	712/200
135	US 6006013 A	☒	Object optimized printing system and method	358/1.15
136	US 5996070 A	☒	Microprocessor capable of executing condition execution instructions using encoded condition execution field in the instructions	712/236
137	US 5978592 A	☒	Video decompression and decoding system utilizing control and data tokens	712/1
138	US 5956741 A	☒	Interface for connecting a bus to a random access memory using a swing buffer and a buffer manager	711/1
139	US 5956519 A	☒	Picture end token in a system comprising a plurality of pipeline stages	712/16
140	US 5941984 A	☒	Data processing device	712/218
141	US 5933651 A	☒	Programmable controller	712/42
142	US 5933618 A	☒	Speculative register storage for storing speculative results corresponding to register updated by a plurality of concurrently recorded instruction	712/217
143	US 5922069 A	☒	Reorder buffer which forwards operands independent of storing destination specifiers therein	712/217
144	US 5915109 A	☒	Microprocessor for processing a saturation instruction of an optional-bit length value	712/221
145	US 5907682 A	☒	Communication LSI for responding to future supplements and modifications of the standard	709/230
146	US 5898621 A	☒	Batch erasable single chip nonvolatile memory device and erasing method therefor	365/185.33
147	US 5892923 A	☒	Parallel computer system using properties of messages to route them through an interconnect network and to select virtual channel circuits therewithin	709/239
148	US 5881301 A	☒	Inverse modeller	712/1
149	US 5872989 A	☒	Processor having a register configuration suited for parallel execution control of loop processing	712/23
150	US 5872964 A	☒	Comparison operating unit and graphic operating system	712/234
151	US 5870580 A	☒	Decoupled forwarding reorder buffer configured to allocate storage in chunks for instructions having unresolved dependencies	712/218
152	US 5867696 A	☒	Saving a program counter value as the return address in an arbitrary general purpose register	712/233
153	US 5860026 A	☒	Information processing system for controlling operations of input/output devices of another clusters according to control instructions issued from a cluster	710/33
154	US 5859926 A	☒	Device and method for data coding and decoding	382/166

	Document ID	U	Title	Current OR
155	US 5844843 A	☒	Single chip data processing apparatus having a flash memory which is rewritable under the control of built-in CPU in the external write mode	365/185.24
156	US 5842033 A	☒	Padding apparatus for passing an arbitrary number of bits through a buffer in a pipeline system	712/1
157	US 5841731 A	☒	Semiconductor device having externally settable operation mode	365/233
158	US 5838896 A	☒	Central processing unit for preventing program malfunction	714/23
159	US 5835740 A	☒	Data pipeline system and data encoding method	712/200
160	US 5815698 A	☒	Microprocessor having delayed instructions	712/237
161	US 5812809 A	☒	Data processing system capable of execution of plural instructions in parallel	712/212
162	US 5809252 A	☒	Data processing system, memory access device and method including selecting the number of pipeline stages based on pipeline conditions	711/169
163	US 5809270 A	☒	Inverse quantizer	712/200
164	US 5805914 A	☒	Data pipeline system and data encoding method	382/232
165	US 5802338 A	☒	Method of self-parallelizing and self-parallelizing multiprocessor using the method	712/217
166	US 5784631 A	☒	Huffman decoder	382/246
167	US 5778208 A	☒	Flexible pipeline for interlock removal	712/203
168	US 5768561 A	☒	Tokens-based adaptive video processing arrangement	710/63
169	US 5764941 A	☒	Operating circuit and method for processing signals in ADPCM system	712/209
170	US 5761490 A	☒	Changing the meaning of a pre-decode bit in a cache memory depending on branch prediction mode	712/239
171	US 5748873 A	☒	Fault recovering system provided in highly reliable computer system having duplicated processors	714/11
172	US 5745723 A	☒	Data processing system capable of execution of plural instructions in parallel	712/212
173	US 5737020 A	☒	Adaptive field/frame encoding of discrete cosine transform	375/240.2
174	US 5729500 A	☒	Draw with variable internal operation frequency	365/230.01
175	US 5724548 A	☒	System including processor and cache memory and method of controlling the cache memory	711/138
176	US 5724537 A	☒	Interface for connecting a bus to a random access memory using a two wire link	711/1
177	US 5715440 A	☒	Branch instruction executing device for tracing branch instruments based on instruction type	712/233

	Document ID	U	Title	Current OR
178	US 5692170 A	☒	Apparatus for detecting and executing traps in a superscalar processor	712/244
179	US 5687345 A	☒	Microcomputer having CPU and built-in flash memory that is rewritable under control of the CPU analyzing a command supplied from an external device	711/103
180	US 5687303 A	☒	Printer controller for object optimized printing	358/1.18
181	US 5685010 A	☒	Data transfer control device for controlling data transfer between shared memories of network clusters	712/28
182	US 5649229 A	☒	Pipeline data processor with arithmetic/logic unit capable of performing different kinds of calculations in a pipeline stage	712/24
183	US 5644504 A	☒	Dynamically partitionable digital video encoder processor	382/248
184	US 5634136 A	☒	Data processor and method of controlling the same	712/237
185	US 5632023 A	☒	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218
186	US 5628024 A	☒	Computer architecture capable of concurrent issuance and execution of general purpose multiple instructions	712/23
187	US 5615349 A	☒	Data processing system capable of execution of plural instructions in parallel	712/212
188	US 5603012 A	☒	Start code detector	712/208
189	US 5598368 A	☒	Batch erasable nonvolatile memory device and erasing method	365/185.01
190	US 5596760 A	☒	Program control method and program control apparatus	712/241
191	US 5581774 A	☒	Data processor decoding and executing a train of instructions of variable length at increased speed	712/210
192	US 5579500 A	☒	Control apparatus for controlling data read accesses to memory and subsequent address generation scheme based on data/memory width determination and address validation	711/220
193	US 5579498 A	☒	Pipelined data processing system capable of stalling and resuming a pipeline operation without using an interrupt processing	712/245
194	US 5539900 A	☒	Information processing system	703/26
195	US 5526054 A	☒	Apparatus for header generation	348/467
196	US 5524088 A	☒	Multi-functional operating circuit providing capability of freely combining operating functions	708/493
197	US 5511172 A	☒	Speculative execution processor	712/235
198	US 5506970 A	☒	Bus arbitrator circuit	710/113
199	US 5488710 A	☒	Cache memory and data processor including instruction length decoding circuitry for simultaneously decoding a plurality of variable length instructions	711/125
200	US 5483657 A	☐	Method of controlling execution of a data flow program and apparatus therefor	712/27

	Document ID	U	Title	Current OR
1	JP 20032 42799 A	☐	SEMICONDUCTOR INTEGRATED CIRCUIT	
2	JP 20020 14809 A	☒	MICROPROCESSOR AND ASSEMBLER AND ITS METHOD AND RECORDING MEDIUM WITH ITS PROGRAM RECORDED	
3	JP 20013 44100 A	☒	CENTRAL PROCESSING UNIT EQUIPPED WITH PLURAL FLAG REGISTERS	
4	JP 20011 75470 A	☒	DATA PROCESSOR	
5	JP 20001 37619 A	☒	MICROCOMPUTER	
6	JP 11177 653 A	☒	MPEG DATA MSFER CONTROL CIRCUIT	
7	JP 11136 207 A	☒	RECEPTION SIGNAL CORRECTION SYSTEM AND ORTHOGONAL FREQUENCY DIVISION MULTIPLEX SIGNAL TRANSMITTER	
8	JP 11031 105 A	☒	DEVICE AND METHOD FOR PRODUCING DATA CAPSULE	
9	JP 11015 590 A	☒	PERSONAL COMPUTER SYSTEM	
10	JP 10224 147 A	☒	FREQUENCY-ADJUSTING DEVICE OF OSCILLATOR CIRCUIT	
11	JP 10224 146 A	☒	FREQUENCY-ADJUSTING DEVICE FOR OSCILLATOR CIRCUIT	
12	JP 10105 396 A	☒	PROCESSOR	
13	JP 10050 055 A	☒	SEMICONDUCTOR MEMORY AND DATA PROCESSOR	
14	JP 09311 786 A	☒	DATA PROCESSOR	
15	JP 08222 996 A	☒	AUTOMATIC CHANNEL SELECTION METHOD FOR RADIO BROADCAST	
16	JP 08153 000 A	☒	INSTRUCTION PROCESSOR	
17	JP 07154 677 A	☒	IMAGE PICKUP DEVICE	
18	JP 06290 078 A	☒	MICROPROCESSOR	
19	JP 05265 912 A	☒	COMMAND CODE ISSUING METHOD	
20	JP 05252 119 A	☒	SAMPLING FREQUENCY CONVERTER	
21	JP 05224 928 A	☒	DATA PROCESSOR	

	Document ID	U	Title	Current OR
22	JP 05165 629 A	☒	MICROPROCESSOR	
23	JP 05012 010 A	☒	BRANCH FORECAST SYSTEM	
24	JP 05012 008 A	☒	CENTRAL ARITHMETIC PROCESSING UNIT	
25	JP 04353 925 A	☒	ARITHMETIC UNIT	
26	JP 04328 644 A	☒	DEBUG BACK-UP DEVICE	
27	JP 04288 688 A	☒	BIT MAP DISPLAY CONTROLLER	
28	JP 04273 529 A	☒	PARALLEL ARITHMETIC CIRCUIT	
29	JP 04162 156 A	☒	INFORMATION PROCESSOR	
30	JP 04062 637 A	☒	MICROPROCESSOR	
31	JP 04035 180 A	☒	REPRODUCTION INFORMATION DISPLAY DEVICE	
32	JP 04000 515 A	☒	CLOCK SUPPLYING SYSTEM AND ARITHMETIC PROCESSOR	
33	JP 03149 622 A	☒	DATA PROCESSOR	
34	JP 03132 843 A	☒	MICROPROCESSOR	
35	JP 03095 629 A	☒	DATA PROCESSOR	
36	JP 01309 129 A	☒	MICROPROCESSOR	
37	JP 01261 780 A	☒	STORAGE CONTROL SYSTEM	
38	JP 01106 244 A	☒	VIRTUAL STORAGE DEVICE	
39	JP 01036 334 A	☒	MICROCOMPUTER	
40	JP 63208 142 A	☒	INFORMATION PROCESSOR	
41	JP 63036 432 A	☒	FLOATING POINT ARITHMETIC UNIT	
42	JP 62285 137 A	☒	DIGITAL SIGNAL PROCESSOR	
43	JP 62224 828 A	☒	INFORMATION PROCESSOR	
44	JP 62119 638 A	☒	DATA PROCESSING SYSTEM	

	Document ID	U	Title	Current OR
45	JP 62044 834 A	☒	CONTROL SYSTEM FOR ELECTRONIC COMPUTER	
46	JP 60114 972 A	☒	FORM FORMAT FORMING DEVICE	
47	JP 56074 749 A	☒	MICROPROGRAM CONTROLLING DEVICE	
48	WO 98137 59 A1	☒	DATA PROCESSOR AND DATA PROCESSING SYSTEM	
49	JP 20030 85509 A	☒	Memory card for personal computer, has process unit that detects whether received command is effective, based on decoding result of command and set index value	
50	US 20020 17430 0 A	☒	Data processor pre-codes advanced instruction portion of instruction data before instruction data is processed and loads instruction codes required for processing into cache memory based on pre-decoding results	
51	EP 11681 29 A	☒	Microcontroller with variable instruction coding has decoder designed to decode at least one conditional instruction so result of decoding this instruction depends on contents of memory	
52	JP 20013 44100 A	☒	Central processing unit stores condition of calculation result of decoded input command in several flag registers whose branch conditions are judged based on stored result	
53	JP 20012 65751 A	☒	Microcomputer device for mobile-communication apparatus, changes operation condition of device based on command data decoding result	
54	WO 20014 2903 A	☒	Data processing apparatus for executing specific load instruction in which converter circuit converts integer data whose bit length is shorter than bit length of floating-point data register	
55	JP 20011 09626 A	☒	Pipeline calculating unit in computer system, has instruction decoder decoding instructions published to calculator to store result in downstream latch based on data held by upstream latch	
56	JP 20010 14160 A	☒	Information processor for pipeline architecture, outputs instruction reading demand to memory based on result of preset instruction decoder	
57	JP 11275 205 A	☒	Aural command based telephone number dialing system in telephone - has speech recognition unit which recognizes decoded input phonation among stored results and displays best decoding result for dial operation	
58	JP 11232 170 A	☒	Instruction memory extension apparatus for semiconductor device - has memory control unit for memory operation, based on starting signal and memory extension control unit for memory space based on completion instruction	
59	JP 11191 088 A	☒	External auxiliary memory for computer system - has two device bus control units which respectively access data unit depending on decoding result from two input output command process units	
60	JP 11154 393 A	☒	Non-volatile semiconductor memory e.g. electrically erasable programmable read only memory EEPROM, used for recording of multimedia information - has controller which makes predetermined number as designated page unit when predetermined command for designating program unit is included based on decoding result of command decoder	
61	JP 11024 929 A	☒	Calculation processing apparatus - has selector that chooses one instruction from simultaneously fetched instructions, and outputs chosen instruction to decoder based on decision result of branch conditions about branch instruction	
62	US 58260 97 A	☒	Data driven information processing - involves subjecting data packets to specified operation processing based on its decoded instruction result and adding operation processing results, cumulatively	

	Document ID	U	Title	Current OR
63	JP 10161871 A	☒	Processor architecture e.g. for microprocessor, signal processor - has instruction decoder which outputs control signal to forward data depending on condition judging result, when input instruction is data forwarding instruction	
64	WO 9813759 A	☒	Data processor and data processing system - provides task buffers with program storage area and pointer for successively reading out instructions selected through selector, and controls selection by switching controller in accordance with internally or externally-generated event	
65	JP 10050055 A	☒	Semiconductor memory for computer system, e.g. SGRAM - has input data controllers which facilitate simultaneous write-in of data in several column addresses of memory cell array based on decoded form of data block write command	
66	JP 08241296 A	☒	semiconductor IC with built-in synchronous memory for processing data - has precharge control part which deters generation of precharge demand signal, when first and second prohibition signals show that decoding result is invalid	
67	EP 582991 A	☒	Data processing circuit with CPU and inbuilt electrically rewritable non-volatile flash memory in single substrate - includes command latch made externally writable, command analyser and sequence controller	
68	EP 561271 A	☒	Microcomputer with non-volatile flash memory with writable information - has central processor with multiple memory blocks of different capacities, switched between operation modes when rewriting memory	
69	EP 417013 A	☒	Data processor decoding and executing train of instructions - stores prefetched instruction code, and sequentially outputs instruction with units of set number of bits	
70	SU 1628215 A	☒	Transceiver for communication engineering - has signal input of error analyser on transmission side connected to error output of decoder and signal input of matching unit	
71	EP 399762 A	☒	Multiple instruction issue computer architecture - has series of pipeline stages and includes resources for accepting family of instructions at each stage	
72	EP 374370 A	☒	Non exclusive cache lines storage in multiprocessor systems - by allowing instruction execution to continue without result commitment until cache line made exclusive	
73	EP 301220 A	☒	Computer system allowing out of sequence instruction execution - executes instruction register array using processor store and hardware register	
74	SU 1176334 A	☐	Programmes and micro-programmes tester - has input taken via OR=gates to address counter with output taken to memory and register	

	L #	Hits	Search Text	DBs
1	L1	13	(result meaning) near10 decod$3 near10 (instruction command) near20 (depend$3 based alter$3 modif$6 chang$3) near10 mode near10 (flag bit register)	USPAT; US-PGPUB
2	L3	24	decod$3 near10 (instruction command) near20 (depend$3 based alter$3 modif$6 chang$3) near10 mode near10 (flag bit register)	EPO; JPO; DERWENT; IBM_TDB
3	L2	91	decod$3 near10 (instruction command) near20 (depend$3 based alter$3 modif$6 chang$3) near10 mode near10 (flag bit register)	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	JP 20010 35158 A	☐	METHOD AND SYSTEM FOR ACCESSING MEMORY	
2	JP 10171 441 A	☐	CHARACTER DISPLAY CONTROL CIRCUIT	
3	JP 08234 979 A	☐	PROCESSOR HAVING BRANCH INSTRUCTION EXECUTING FUNCTION AND BRANCH INSTRUCTION CONTROL METHOD	
4	JP 04254 985 A	☐	DRAM CONTROLLER	
5	JP 04102 982 A	☐	MICROCOMPUTER	
6	JP 01283 647 A	☐	DUPLICATED ERROR GENERATING DEVICE FOR MICROPROCESSOR	
7	JP 01037 627 A	☐	REGISTER UPDATING MECHANISM	
8	JP 60096 030 A	☐	DECODING SYSTEM	
9	JP 59003 642 A	☐	CONTROL REGISTER PROCESSING SYSTEM	
10	JP 57059 205 A	☐	NUMERIC CONTROLLER	
11	JP 56074 749 A	☐	MICROPROGRAM CONTROLLING DEVICE	
12	DE 19932 465 C1	☐	Arrangement for programming functional devices equipped with digital decoders changes decoder to programming mode using drive voltage on track with digital controller in reset state	
13	EP 10507 98 A1	☐	Decoding instructions	
14	DE 19932 465 C	☐	Arrangement for programming functional devices equipped with digital decoders changes decoder to programming mode using drive voltage on track with digital controller in reset state	
15	EP 10507 98 A	☐	Decode unit for decoding instructions in a processor that can support three instruction modes has detector that temporarily allows first length instructions to be decoded without changing instruction mode held in register	
16	US 60121 38 A	☐	Dynamically variable length CPU pipeline for executing multiple instruction sets	
17	JP 11154 393 A	☐	Non-volatile semiconductor memory e.g. electrically erasable programmable read only memory EEPROM, used for recording of multimedia information - has controller which makes predetermined number as designated page unit when predetermined command for designating program unit is included based on decoding result of command decoder	
18	US 58023 60 A	☐	Integrated circuit with digital processor for dynamic selection of instruction execution intervals - has decode stage coupled to execute stage with mode input for selecting number of clock cycles taken to execute flag-modifying instruction	
19	US 51230 96 A	☐	Data processor with addressing mode decoding function - modifies entry address of microinstruction when addressing mode of operand detected to enable entry address	
20	JP 02011 076 A	☐	Sound decoder for MUSE television receiver - operates muting circuit when state change of mode command bit in control code is detected NoAbstract Dwg 0/2	

	Document ID	U	Title	Current OR
21	DE 3500741 A	☐	Integrated circuit for floppy disc drive control - has registers to handle control and data transfers between disc drive and computer operating with status interlock stage	
22	SU 1065852 A	☐	Multi-computer network computer interfacing unit - has memory data input coupled through high-way with coupling amplifier data outputs to group lines	
23	WO 8303017 A	☐	Computer with static cache - automatically maps memory contents into machine registers during program execution	
24	EP 40703 A	☐	Enhancement of 370 type data processor - reduces overhead incurred by multiple users by permitting program in one address space to obtain access to data in another address space	

	Document ID	U	Title	Current OR
1	US 20030021163 A1	☐	Semiconductor memory device and information device	365/189.12
2	US 20010007541 A1	☐	Semiconductor memory device	365/233
3	US 20010005132 A1	☐	Semiconductor device testing method and system and recording medium	324/158.1
4	US 6617842 B2	☐	Semiconductor device testing method and system employing trace data	324/158.1
5	US 6549475 B2	☐	Semiconductor memory device and information device	365/189.12
6	US 6504789 B2	☐	Semiconductor memory device	365/233
7	US 6425047 B1	☐	Process containing address decoders suited to improvements in clock speed	711/101
8	US 5761490 A	☐	Changing the meaning of a pre-decode bit in a cache memory depending on branch prediction mode	712/239
9	US 5506970 A	☐	Bus arbitrator circuit	710/113
10	US 5412784 A	☐	Apparatus for parallelizing serial instruction sequences and creating entry points into parallelized instruction sequences at places other than beginning of particular parallelized instruction sequence	712/245
11	US 5408658 A	☐	Self-scheduling parallel computer system and method	712/216
12	US 5347639 A	☐	Self-parallelizing computer system and method	712/203
13	US 4414622 A	☐	Addressing system for a computer, including a mode register	711/215

	Document ID	U	Title	Current OR
1	US 20040019756 A1	☐	Memory device supporting a dynamically configurable core organization	711/170
2	US 20030223293 A1	☒	Synchronous type semiconductor memory device	365/200
3	US 20030164510 A1	☒	Redundancy architecture for repairing semiconductor memories	257/200
4	US 20030135779 A1	☒	Microprocessor	713/600
5	US 20030126529 A1	☒	Wafer burn-in test mode circuit	714/720
6	US 20030101333 A1	☒	Data processor	712/226
7	US 20030085731 A1	☒	Semiconductor device having test mode entry circuit	326/16
8	US 20030081491 A1	☒	SEMICONDUCTOR MEMORY DEVICE WITH REDUCED POWER CONSUMPTION	365/233
9	US 20030075789 A1	☒	Semiconductor storage device having memory chips in a stacked structure	257/678
10	US 20030061536 A1	☒	Power controlling method for semiconductor storage device and semiconductor storage device employing same	714/14
11	US 20030021163 A1	☐	Semiconductor memory device and information device	365/189.12
12	US 20030014457 A1	☒	Method and apparatus for vector processing	708/520
13	US 20020171075 A1	☒	Register setting method and semiconductor device	257/10
14	US 20020145929 A1	☒	Control circuit and semiconductor memory device	365/222
15	US 20010023424 A1	☒	Exponent unit of data processing system	708/277
16	US 20010007541 A1	☐	Semiconductor memory device	365/233
17	US 20010005132 A1	☐	Semiconductor device testing method and system and recording medium	324/158.1

	Document ID	U	Title	Current OR
18	US 6678818 B1	☒	Decoding next instruction of different length without length mode indicator change upon length change instruction detection	712/210
19	US 6675290 B1	☒	Processor for improving instruction utilization using multiple parallel processors and computer system equipped with the processor	712/229
20	US 6651196 B1	☒	Semiconductor device having test mode entry circuit	714/724
21	US 6631463 B1	☒	Method and apparatus for patching problematic instructions in a microprocessor using software interrupts	712/227
22	US 6617842 B2	☐	Semiconductor device testing method and system employing trace data	324/158.1
23	US 6577550 B2	☒	Control circuit and semiconductor memory device	365/222
24	US 6574727 B1	☒	Method and apparatus for instruction sampling for performance monitoring and debug	712/227
25	US 6566760 B1	☒	Semiconductor storage device having memory chips in a stacked structure	257/777
26	US 6552955 B1	☒	Semiconductor memory device with reduced power consumption	365/233
27	US 6549491 B1	☒	Pipelined SDRAM memory controller to optimize bus utilization	711/158
28	US 6549475 B2	☐	Semiconductor memory device and information device	365/189.12
29	US 6539502 B1	☒	Method and apparatus for identifying instructions for performance monitoring in a microprocessor	714/47
30	US 6504789 B2	☐	Semiconductor memory device	365/233
31	US 6492992 B2	☒	Graphic pattern processing apparatus	345/568
32	US 6487629 B1	☒	Semiconductor memory for operation in a plurality of operational modes	711/104
33	US 6463518 B1	☒	Generation of memory addresses for accessing a memory utilizing scheme registers	711/220
34	US 6453278 B1	☒	Flexible implementation of a system management mode (SMM) in a processor	703/27
35	US 6426560 B1	☒	Semiconductor device and memory module	257/777
36	US 6425047 B1	☐	Process containing address decoders suited to improvements in clock speed	711/101
37	US 6414530 B2	☒	Semiconductor integrated circuit device, semiconductor memory system and clock synchronous circuit	327/269
38	US 6381720 B1	☒	Test circuit and method for system logic	714/727
39	US 6381690 B1	☒	Semiconductor memory device in which use of cache can be selected	365/230.03
40	US 6336178 B1	☒	RISC86 instruction set	712/23

	Document ID	U	Title	Current OR
41	US 6292848 B1	☒	Computing system adapter card for supporting legacy and plug and play configurations	710/8
42	US 6208563 B1	☒	Semiconductor memory device which continuously performs read/write operations with short access time	365/189.05
43	US 6141742 A	☒	Method for reducing number of bits used in storage of instruction address pointer values	711/220
44	US 6093213 A	☒	Flexible implementation of a system management mode (SMM) in a processor	703/27
45	US 6085314 A	☒	Central processing unit including APX and DSP cores and including selectable APX and DSP execution modes	712/213
46	US 6081886 A	☒	Holding mechanism for changing operation modes in a pipelined computer	712/229
47	US 6032247 A	☒	Central processing unit including APX and DSP cores which receives and processes APX and DSP instructions	712/35
48	US 6014714 A	☒	Adapter card system including for supporting multiple configurations using mapping bit	710/8
49	US 5991531 A	☒	Scalable width vector processor architecture for efficient emulation	703/26
50	US 5973988 A	☒	Semiconductor memory device having circuit for monitoring set value of mode register	365/230.08
51	US 5926642 A	☒	RISC86 instruction set	712/1
52	US 5925123 A	☒	Processor for executing instruction sets received from a network or from a local memory	712/212
53	US 5920713 A	☒	Instruction decoder including two-way emulation code branching	712/236
54	US 5909567 A	☒	Apparatus and method for native mode processing in a RISC-based CISC processor	712/208
55	US 5893927 A	☒	Memory device having programmable device width, method of programming, and method of setting device width for memory device	711/171
56	US 5854913 A	☒	Microprocessor with an architecture mode control capable of supporting extensions of two distinct instruction-set architectures	712/210
57	US 5852428 A	☒	Display driving device	345/100
58	US 5819056 A	☒	Instruction buffer organization method and system	712/204
59	US 5809273 A	☒	Instruction predecode and multiple instruction decode	712/210
60	US 5802360 A	☒	Digital microprocessor device having dnamically selectable instruction execution intervals	712/229
61	US 5794063 A	☒	Instruction decoder including emulation using indirect specifiers	712/23
62	US 5793775 A	☒	Low voltage test mode operation enable scheme with hardware safeguard	714/724
63	US 5781750 A	☒	Dual-instruction-set architecture CPU with hidden software emulation mode	712/209

	Document ID	U	Title	Current OR
64	US 5761490 A	☐	Changing the meaning of a pre-decode bit in a cache memory depending on branch prediction mode	712/239
65	US 5703616 A	☒	Display driving device	345/98
66	US 5663745 A	☒	Display driving device	345/98
67	US 5636173 A	☒	Auto-precharge during bank selection	365/230.03
68	US 5630161 A	☒	Serial-parallel digital signal processor	712/36
69	US 5560036 A	☒	Data processing having incircuit emulation function	712/227
70	US 5530804 A	☒	Superscalar processor with plural pipelined execution units each unit selectively having both normal and debug modes	714/30
71	US 5506970 A	☐	Bus arbitrator circuit	710/113
72	US 5412784 A	☐	Apparatus for parallelizing serial instruction sequences and creating entry points into parallelized instruction sequences at places other than beginning of particular parallelized instruction sequence	712/245
73	US 5408658 A	☐	Self-scheduling parallel computer system and method	712/216
74	US 5396498 A	☒	Integrated circuit with peripheral test controller	714/703
75	US 5347639 A	☐	Self-parallelizing computer system and method	712/203
76	US 5280593 A	☒	Computer system permitting switching between architected and interpretation instructions in a pipeline by enabling pipeline drain	712/208
77	US 5226164 A	☒	Millicode register management and pipeline reset	712/209
78	US 5167026 A	☒	Simultaneously or sequentially decoding multiple specifiers of a variable length pipeline instruction based on detection of modified value of specifier registers	712/210
79	US 5148528 A	☒	Method and apparatus for simultaneously decoding three operands in a variable length instruction when one of the operands is also of variable length	712/210
80	US 5142633 A	☒	Preprocessing implied specifiers in a pipelined processor	712/225
81	US 5129079 A	☒	Computer system having subinstruction surveillance capability	712/211
82	US 5123096 A	☒	Data processor with addressing mode decoding function	712/212
83	US 5031096 A	☒	Method and apparatus for compressing the execution time of an instruction stream executing in a pipelined processor	711/169
84	US 4561443 A	☒	Coherent inductive communications link for biomedical applications	607/31
85	US 4414622 A	☐	Addressing system for a computer, including a mode register	711/215

	Document ID	U	Title	Current OR
86	US 4344129 A	☒	Data processor system capable of providing both a computer mode and a sequencer mode of operation	712/229
87	US 4199810 A	☒	Radiation hardened register file	714/15
88	US 4107781 A	☒	Electronic calculator or microprocessor with indirect addressing	708/100
89	US 4084235 A	☒	Emulation apparatus	703/26
90	US 3818460 A	☒	EXTENDED MAIN MEMORY ADDRESSING APPARATUS	711/2
91	US 3577190 A	☐	APPARATUS IN A DIGITAL COMPUTER FOR ALLOWING THE SKIPPING OF PREDETERMINED INSTRUCTIONS IN A SEQUENCE OF INSTRUCTIONS, IN RESPONSE TO THE OCCURRENCE OF CERTAIN CONDITIONS	712/226

	L #	Hits	Search Text	DBs
1	L1	611	decod$3 near10 (condition$3 near5 (instruction command) not (branch adj instruction))	USPAT; US-PGPUB
2	L2	613	decod$3 near10 (conditional near5 (instruction command))	USPAT; US-PGPUB
3	L3	71	decod$3 near10 (conditional adj (instruction command))	USPAT; US-PGPUB
4	L4	46	3 near30 (memory register storage)	USPAT; US-PGPUB
5	L5	21	1 near10 (depend$3 result) near30 (memory register storage)	USPAT; US-PGPUB
6	L6	1921	decod$3 near10 (instruction command) near10 (modif$6 chang$3 alter$3)	USPAT; US-PGPUB
7	L7	750	6 near20 (register memory storage flag)	USPAT; US-PGPUB
8	L9	58	7 near10 (result meaning depend$3)	USPAT; US-PGPUB
9	L8	72	7 near10 (result meaning depend$3 based)	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20030 22600 2 A1	☐	Devices, systems and methods for conditional instructions notice	712/234
2	US 20030 10579 3 A1	☐	Long instruction word controlling plural independent processor operations	708/625
3	US 20020 04043 0 A1	☐	Microcontroller	712/234
4	US 66812 80 B1	☐	Interrupt control apparatus and method separately holding respective operation information of a processor preceding a normal or a break interrupt	710/261
5	US 65164 07 B1	☐	Information processor	712/226
6	US 64272 05 B1	☐	Digital signal processor and processor reducing the number of instructions upon processing condition execution instructions	712/226
7	US 63453 55 B1	☐	Method and apparatus for distributing commands to a plurality of circuit blocks	712/215
8	US 63341 81 B1	☐	DSP with wait state registers having at least two portions	712/38
9	US 63112 64 B1	☐	Digital signal processor with wait state register	712/38
10	US 62634 19 B1	☐	Integrated circuit with wait state registers	712/38
11	US 62634 18 B1	☐	Process of operating a microprocessor to use wait state numbers	712/38
12	US 62533 07 B1	☐	Data processing device with mask and status bits for selecting a set of status conditions	712/209
13	US 62498 60 B1	☐	System with wait state registers	712/38
14	US 62498 59 B1	☐	IC with wait state registers	712/38
15	US 62471 11 B1	☐	System with wait state register	712/38
16	US 62438 01 B1	☐	System with wait state registers	712/38
17	US 62405 05 B1	☐	System with wait state registers	712/38
18	US 62405 04 B1	☐	Process of operating a microprocessor to change wait states	712/38
19	US 61345 78 A	☐	Data processing device and method of operation with context switching	718/100
20	US 60853 36 A	☐	Data processing devices, systems and methods with mode driven stops	714/30
21	US 60527 76 A	☐	Branch operation system where instructions are queued until preparations is ascertained to be completed and branch distance is considered as an execution condition	712/233
22	US 59464 83 A	☐	Devices, systems and methods for conditional instructions	712/223

	Document ID	U	Title	Current OR
23	US 5907714 A	☐	Method for pipelined data processing with conditioning instructions for controlling execution of instructions without pipeline flushing	712/23
24	US 5829054 A	☐	Devices and systems with parallel logic unit operable on data memory locations	711/202
25	US 5828577 A	☐	Devices and systems with protective terminal configuration, and methods	716/4
26	US 5777885 A	☐	Devices and systems with protective terminal configuration, and methods	716/1
27	US 5724248 A	☐	Devices and systems with protective terminal configuration, and methods	716/4
28	US 5687339 A	☐	Pre-reading and pre-decoding of instructions of a microprocessor within single cycle	712/207
29	US 5652910 A	☐	Devices and systems with conditional instructions	712/218
30	US 5617574 A	☐	Devices, systems and methods for conditional instructions	712/200
31	US 5586275 A	☐	Devices and systems with parallel logic unit operable on data memory locations, and methods	712/223
32	US 5583767 A	☐	Devices and systems with parallel logic unit, and methods notice	701/1
33	US 5579497 A	☐	Devices and systems with parallel logic unit, and methods	375/222
34	US 5579218 A	☐	Devices and systems with parallel logic unit, and methods	700/1
35	US 5550993 A	☐	Data processor with sets of two registers where both registers receive identical information and when context changes in one register the other register remains unchanged	712/229
36	US 5509129 A	☐	Long instruction word controlling plural independent processor operations	712/203
37	US 5383196 A	☐	SONET signal generating apparatus and method	714/712
38	US 5349687 A	☐	Speech recognition system having first and second registers enabling both to concurrently receive identical information in one context and disabling one to retain the information in a next context	704/231
39	US 5319792 A	☐	Modem having first and second registers enabling both to concurrently receive identical information in one context and disabling one to retain the information in a next context	712/228
40	US 5319789 A	☐	Electromechanical apparatus having first and second registers enabling both to concurrently receive identical information in one context and disabling one to retain the information in a next context	712/228
41	US 5313648 A	☐	Signal processing apparatus having first and second registers enabling both to concurrently receive identical information in one context and disabling one to retain the information in a next context	712/228
42	US 5155812 A	☐	Devices and method for generating and using systems, software waitstates on address boundaries in data processing	710/59
43	US 5142677 A	☐	Context switching devices, systems and methods	718/108
44	US 5072418 A	☐	Series maxium/minimum function computing devices, systems and methods	708/207

	Document ID	U	Title	Current OR
45	US 4598358 A	☐	Pipelined digital signal processor using a common data and control bus	712/35
46	US 4539635 A	☐	Pipelined digital processor arranged for conditional operation	712/234

	Document ID	U	Title	Current OR
1	US 20030 18258 9 A1	☐	Instruction conversion apparatus and instruction conversion method providing power control information, program and circuit for implementing the instruction conversion, and microprocessor for executing the converted instruction	713/300
2	US 20020 04043 0 A1	☐	Microcontroller	712/234
3	US 20020 03572 4 A1	☐	Data rate conversion	725/1
4	US 66788 19 B1	☐	Pipeline microprocessor with conditional jump in one clock cycle	712/219
5	US 64272 05 B1	☐	Digital signal processor and processor reducing the number of instructions upon processing condition execution instructions	712/226
6	US 63269 99 B1	☐	Data rate conversion	348/441
7	US 60264 80 A	☐	Processor having bug avoidance function and method for avoiding bug in processor	712/37
8	US 59580 48 A	☐	Architectural support for software pipelining of nested loops	712/241
9	US 57649 41 A	☐	Operating circuit and method for processing signals in ADPCM system	712/209
10	US 52533 49 A	☐	Decreasing processing time for type 1 dyadic instructions	712/223
11	US 49597 80 A	☐	Microprogram processor with logic circuitry for combining signals from a microcode decoder and an instruction code decoder to produce a memory access signal	712/212
12	US 47195 63 A	☐	Data transmission control device for controlling transfer of large amounts of data between two memory units	711/165
13	US 45983 58 A	☐	Pipelined digital signal processor using a common data and control bus	712/35
14	US 45396 35 A	☐	Pipelined digital processor arranged for conditional operation	712/234
15	US 42518 59 A	☐	Data processing system with an enhanced pipeline control	712/219
16	US 40259 02 A	☐	General purpose sequence controller	700/18
17	US 39097 99 A	☐	Microprogrammable peripheral processing system	712/234
18	US 38497 65 A	☐	PROGRAMMABLE LOGIC CONTROLLER	712/246
19	US 38326 96 A	☐	GENERAL PURPOSE SEQUENCE CONTROLLER	700/9
20	US 37365 66 A	☐	CENTRAL PROCESSING UNIT WITH HARDWARE CONTROLLED CHECKPOINT AND RETRY FACILITIES	714/15
21	US 35789 18 A	☐	COMPUTER CONTROLLED SWITCHING SYSTEM USING FLIP-FLOPS FOR CONTROL OF REPETITIVE OPERATIONS	379/280

	Document ID	U	Title	Current OR
1	US 20040 00321 4 A1	☐	Instruction control method and processor	712/234
2	US 20040 00320 7 A1	☐	Program counter control method and processor	712/218
3	US 20030 20465 2 A1	☐	Data transfer control device, electronic equipment and data transfer control method	710/33
4	US 20030 14475 5 A1	☐	Method for processing and reproducing audio signal at desired sound quality, reduced data volume or adjusted output level, apparatus for processing audio signal with sound quality control information or test tone signal or at reduced data volume, recording medium for recording audio signal with sound quality control information or test tone signal or at reduced data volume, and apparatus for reproducing audio signal at desired sound quality, reduced data volume or adjusted output level	700/94
5	US 20030 09365 2 A1	☐	Operand file using pointers and reference counters and a method of use	712/217
6	US 20030 03351 1 A1	☐	Processor having multiple program counters and trace buffers outside an execution pipeline	712/235
7	US 20030 02634 2 A1	☐	Decoding apparatus, decoding method, decoding program, and decoding program storage medium	375/240 .25
8	US 20030 00458 8 A1	☐	Method for processing and reproducing audio signal at desired sound quality, reduced data volume or adjusted output level, apparatus for processing audio signal with sound quality control information or test tone signal or at reduced data volume, recording medium for recording audio signal with sound quality control information or test tone signal or at reduced data volume, and apparatus for reproducing audio signal at desired sound quality, reduced data volume or adjusted output level	700/94
9	US 20020 19445 7 A1	☐	Memory system for ordering load and store instructions in a processor that performs out-of-order multithread execution	712/218
10	US 20020 17107 5 A1	☐	Register setting method and semiconductor device	257/10
11	US 20020 12873 9 A1	☐	Method for processing and reproducing audio signal at desired sound quality, reduced data volume or adjusted output level, apparatus for processing audio signal with sound quality control information or test tone signal or at reduced data volume, recording medium for recording audio signal with sound quality control information or test tone signal or at reduced data volume, and apparatus for reproducing audio signal at desired sound quality, reduced data volume or adjusted output level	700/94
12	US 20020 12381 0 A1	☐	Method for processing and reproducing audio signal at desired sound quality, reduced data volume or adjusted output level, apparatus for processing audio signal with sound quality control information or test tone signal or at reduced data volume, recording medium for recording audio signal with sound quality control information or test tone signal or at reduced data volume, and apparatus for reproducing audio signal at desired sound quality, reduced data	700/94

	Document ID	U	Title	Current OR
13	US 20010 01494 1 A1	☐	Processor having multiple program counters and trace buffers outside an execution pipeline	712/228
14	US 66788 18 B1	☐	Decoding next instruction of different length without length mode indicator change upon length change instruction detection	712/210
15	US 66041 93 B1	☐	Processor in which register number translation is carried out	712/228
16	US 65606 92 B1	☐	Data processing circuit, microcomputer, and electronic equipment	712/23
17	US 65604 97 B2	☐	METHOD FOR PROCESSING AND REPRODUCING AUDIO SIGNAL AT DESIRED SOUND QUALITY, REDUCED DATA VOLUME OR ADJUSTED OUTPUT LEVEL, APPARATUS FOR PROCESSING AUDIO SIGNAL WITH SOUND QUALITY CONTROL INFORMATION OR TEST TONE SIGNAL OR AT REDUCED DATA VOLUME, RECORDING MEDIUM FOR RECORDING AUDIO SIGNAL WITH SOUND QUALITY CONTROL INFORMATION OR TEST TONE SIGNAL OR AT REDUCED DATA VOLUME, AND APPARATUS FOR REPRODUCING AUDIO SIGNAL AT DESIRED SOUND QUALITY, REDUCED DATA VOLUME OR ADJUSTED OUTPUT LEVEL	700/94
18	US 65499 59 B1	☐	Detecting modification to computer memory by a DMA device	710/22
19	US 65359 84 B1	☐	Power reduction for multiple-instruction-word processors with proxy NOP instructions	713/320
20	US 64938 20 B2	☐	Processor having multiple program counters and trace buffers outside an execution pipeline	712/235
21	US 64635 22 B1	☐	Memory system for ordering load and store instructions in a processor that performs multithread execution	712/216
22	US 64569 66 B1	☐	Apparatus and method for decoding audio signal coding in a DSR system having memory	704/212
23	US 64427 01 B1	☐	Power saving by disabling memory block access for aligned NOP slots during fetch of multiple instruction words	713/324
24	US 64272 05 B1	☐	Digital signal processor and processor reducing the number of instructions upon processing condition execution instructions	712/226
25	US 63973 79 B1	☐	Recording in a program execution profile references to a memory-mapped active device	717/140
26	US 63780 61 B1	☐	Apparatus for issuing instructions and reissuing a previous instructions by recirculating using the delay circuit	712/200
27	US 63778 62 B1	☐	Method for processing and reproducing audio signal	700/94
28	US 63082 61 B1	☐	Computer system having an instruction for probing memory latency	712/219
29	US 62405 09 B1	☐	Out-of-pipeline trace buffer for holding instructions that may be re-executed following misspeculation	712/228
30	US 62055 34 B1	☐	Apparatus and method for processing data with a plurality of flag groups	712/32
31	US 61822 10 B1	☐	Processor having multiple program counters and trace buffers outside an execution pipeline	712/235
32	US 61700 82 B1	☐	Taking corrective action in computer programs during instruction processing	717/127

	Document ID	U	Title	Current OR
33	US 6157997 A	☐	Processor and information processing apparatus with a reconfigurable circuit	712/226
34	US 6081886 A	☐	Holding mechanism for changing operation modes in a pipelined computer	712/229
35	US 6073249 A	☐	Information processing system	714/4
36	US 6026480 A	☐	Processor having bug avoidance function and method for avoiding bug in processor	712/37
37	US 6012141 A	☐	Apparatus for detecting and executing traps in a superscalar processor	712/244
38	US 5991868 A	☐	Apparatus and method for processing data with a plurality of flag groups	712/32
39	US 5991531 A	☐	Scalable width vector processor architecture for efficient emulation	703/26
40	US 5917947 A	☐	Image processing method and apparatus permitting use of PDL in compression memory	382/232
41	US 5898621 A	☐	Batch erasable single chip nonvolatile memory device and erasing method therefor	365/185.33
42	US 5895497 A	☐	Microprocessor with pipelining, memory size evaluation, micro-op code and tags	711/169
43	US 5892923 A	☐	Parallel computer system using properties of messages to route them through an interconnect network and to select virtual channel circuits therewithin	709/239
44	US 5872964 A	☐	Comparison operating unit and graphic operating system	712/234
45	US 5835997 A	☐	Information processing system	714/11
46	US 5802338 A	☐	Method of self-parallelizing and self-parallelizing multiprocessor using the method	712/217
47	US 5761490 A	☐	Changing the meaning of a pre-decode bit in a cache memory depending on branch prediction mode	712/239
48	US 5692170 A	☐	Apparatus for detecting and executing traps in a superscalar processor	712/244
49	US 5649229 A	☐	Pipeline data processor with arithmetic/logic unit capable of performing different kinds of calculations in a pipeline stage	712/24
50	US 5632023 A	☐	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218
51	US 5598368 A	☐	Batch erasable nonvolatile memory device and erasing method	365/185.01
52	US 5511172 A	☐	Speculative execution processor	712/235
53	US 5506970 A	☐	Bus arbitrator circuit	710/113
54	US 5481549 A	☐	Apparatus for testing an integrated circuit in which an input test pattern can be changed with an selected application timing	714/744
55	US 5450555 A	☐	Register logging in pipelined computer using register log queue of register content changes and base queue of register log queue pointers for respective instructions	712/228

	Document ID	U	Title	Current OR
56	US 5418917 A	☐	Method and apparatus for controlling conditional branch instructions for a pipeline type data processing apparatus	712/234
57	US 5412784 A	☐	Apparatus for parallelizing serial instruction sequences and creating entry points into parallelized instruction sequences at places other than beginning of particular parallelized instruction sequence	712/245
58	US 5408658 A	☐	Self-scheduling parallel computer system and method	712/216
59	US 5404554 A	☐	Information processing system which converts specific instruction codes to non-user defined instruction codes	712/226
60	US 5396603 A	☐	Data processor having resources and execution start control for starting execution of succeeding instruction in resource before completion of preceding instruction	712/216
61	US 5349671 A	☐	Microprocessor system generating instruction fetch addresses at high speed	712/234
62	US 5347639 A	☐	Self-parallelizing computer system and method	712/203
63	US 5333188 A	☐	Effective address pre-calculation type pipelined microprocessor	711/214
64	US 5167026 A	☐	Simultaneously or sequentially decoding multiple specifiers of a variable length pipeline instruction based on detection of modified value of specifier registers	712/210
65	US 4982283 A	☐	Line-sequential pyramid processing of a plurality of raster-scanned image variables	375/240.12
66	US 4831515 A	☐	Information processing apparatus for determining sequence of parallel executing instructions in response to storage requirements thereof	712/217
67	US 4744043 A	☐	Data processor execution unit which receives data with reduced instruction overhead	708/490
68	US 4456994 A	☐	Remote simulation by remote control from a computer desk	714/33
69	US 4414622 A	☐	Addressing system for a computer, including a mode register	711/215
70	US 4360891 A	☐	Address and data interface unit	712/208
71	US 4138719 A	☐	Automatic writing systems and methods of word processing therefor	358/1.18
72	US 3736566 A	☐	CENTRAL PROCESSING UNIT WITH HARDWARE CONTROLLED CHECKPOINT AND RETRY FACILITIES	714/15